Slot Machine Memory Devices

Week # 5
Overview

• Items to be covered:
  • Memory Devices
    • Terminology
    • General Operation
    • CPU – Memory Connection
  • Read Only Memory (ROM)
    • Overview
    • ROM Architecture
    • Types of ROMs
  • Random Access Memory (RAM)
    • Overview
    • RAM Architecture
Memory Devices

• Terminology
  • Applies to memory devices used in Slot Machines and other computer systems
  • Key Terms
    • Memory Cell, Memory Word, Byte, Nibble, Bit, Capacity, Density, Address, Read Operation, Write Operation, Access Time, Volatile Memory, Random Access Memory (RAM), Sequential Access Memory (SAM), Read Only Memory, Static Memory Devices (e.g., Static RAM – SRAM)
    • Check the book or the on-line learning module for definitions
      • http://sites.csn.edu/jmiller/ET/ET138B/LM-5.htm

• General Memory Operation
  • The internal configurations of the various type of memory may very, but there are common basic operations
Memory Devices

• General Memory Operation

  • Common Operations
    • Input/Output Lines
      • Select memory address that is being accessed for either a Read or Write Operation
      • Select either a read or write operation
      • Supply the input data to be stored during a write operation
      • Hold output data from memory during a read operation
      • Enable/disable memory so it will/will-not respond to address inputs and the read/write command

  • Simplified Operation Example
    • Uses a 4-bit by 32 Word memory
    • Store 32 4-bit words
    • Address lines required:
Memory Devices

• General Memory Operation
  • Simplified Operation Example
    • Since a data word is 4-bits only 4 data lines are needed

• Each word in memory has an address
  • 0 – 31 in decimal or 00000 – 11111 in binary
  • During a read operation the data at the inputs is stored in memory
  • During a write the data in memory is put out on the data outputs
Memory Devices

• General Memory Operation
  • Simplified Operation Example
    • R/W pin controls which operation occurs
      • A logic High enables a Read Operation
      • A logic Low enables a Write Operation
    • Enable pin enables access to the memory
      • A logic High enables the memory for Write and Read Operations
      • A logic Low disables access to memory
  • Writing to address 00011
    • Figure a on the next slide shows an overview of the write operation
  • Reading from address 11110
    • Figure b on the next slide shows an overview of the write operation
Memory Devices

- General Memory Operation
  - Simplified Operation Example

(a) WRITING the data word 0100 into memory location 00011.
(b) READING the data word 1101 from memory location 11110
Memory Devices

• CPU-Memory Connections

  • Overview
    • Semiconductor memory is most of main memory in a slot machine
      • That main memory is in near constant communications w/ the CPU
    • A machine’s main memory is composed of RAM and Rom memory integrated circuit (ICs) chips

  • Interfaced to the CPU over three groups of signal lines
    • Address Bus – shown as one line w/hash - typically 8, 16, 32 lines
Memory Devices

• CPU-Memory Connections
  • Overview
    • Interfaced to the CPU over three groups of signal lines
      • Data Bus – shown as one line w/hash - typically 8, 16, 32 lines
      • Control Bus – shown as one line w/hash
    • The three buses are critical to allow the CPU to read data from memory and to write other info to memory
      • When the machines computer is executing program of instructions
        • The CPU continually fetches info from memory that contains (1) the next instruction (2) the data to be operated upon
        • The CPU will also store (write) data into a particular memory location
  • Busses Defined
    • Address Bus
      • Unidirectional bus between the CPU and the machine’s memory
        • CPU supplies the address
Memory Devices

• CPU-Memory Connections
  • Buses Defined
    • Address Bus
      • Carries a binary address
        • Used to select a memory location
    • Data Bus
      • Bi-directional bus that carries binary data to/from the CPU/memory
      • The CPU acts on the data
      • Memory stores the data
  • Control Bus
    • Uni-directional
      • Carries control signal to the memory or other computer components
  • Read Operation
    • The CPU supplies the binary address of the memory location
      where the data are to be stored.
Memory Devices

• CPU-Memory Connections
  • Write Operation
    • The CPU supplies the binary address of the memory location where the data are to be stored. It places this address on the address bus lines.
    • The CPU places the data to be stored on the data bus lines.
    • The CPU activates the appropriate control signal lines for the memory write operation.
    • The memory ICs decode the binary address to determine which location is being selected for the store operation.
    • The data on the data bus are transferred to the selected memory location.
  • Read Operation
    • The CPU supplies the binary address of the memory location from which data are to be retrieved. It places this address on the address bus lines.
Memory Devices

- **CPU-Memory Connections**
  - **Read Operation**
    - The CPU activates the appropriate control signal lines for the memory read operation.
    - The memory ICs decode the binary address to determine which location is being selected for the read operation.
    - The memory ICs place data from the selected memory location onto the data bus, from where they are transferred to the CPU.
Read Only Memory (ROM)

• Overview
  • Originally intended to hold data that either will not change not change often
    • Still true of most types of ROM
    • What is the exception that is commonly used by many people today? It is an exception to most of what follows.
  • For some ROMs the data is built in at the time of manufacture
  • For others types data is written to ROMs electrically
    • This process is called programming or burning-in
    • Some of the electrically programmable ROMs cannot be changed after the first programming
    • Others can be changed many times
Read Only Memory (ROM)

- ROM Block Diagram
Read Only Memory (ROM)

- ROM Block Diagram
  - Signals Used
    - Addresses
    - Data
    - Control
  - Storage Capacity
    - Has four address lines
      - Thus has $2^4$ (16) addresses
    - Has 8 data lines – thus each address holds one 8-bit word
      - Usually has tri-state buffers which support connections to a bus
      - Thus it is a 16X8 ROM or it stores 16 bytes or data
  - Control Signals
    - This chip only has an Enable control pin
      - Cannot be written to during normal operation
    - This enable pin is called CS or Chip Select NOT
      - Chip Select that is active with a Low logic signal
Read Only Memory (ROM)

- ROM Block Diagram
  - Read Operation
    - Set-up
      - ROM is programmed with the data shown in the table
      - 16 different 8-bit data words are stored at 16 different address locations
    - First the address that is to be read is set on the four address lines
      - \( A_0 \rightarrow A_3 \)
      - Lets use \( 0111_2 \)
    - Then apply a LOW to CS
      - The address is decoded inside of the ROM
      - The data word in location \( 0111_2 \) appears on the \( D_0 \rightarrow D_7 \) pins
        - \( 11101101 \)
      - When CS is held at a logic HIGH the outputs are disabled
Read Only Memory (ROM)

• Types of ROM
  • Key ones covered
    • Mask Programmable, aka, ROM
    • Erasable Programmable ROM, aka, EPROM
    • Electrically Erasable Programmable ROM, aka, EEPROM
    • Flash Memory (heart of USB drives)
  • Mask Programmable, aka, ROM
    • Key characteristics
      • Programmed at time of manufacture with Customers specifications
        • Information is stored in a photographic negative (Mask) that is used during manufacturing
        • Each different set of data stored requires its own Mask
      • Masks are very expensive
Read Only Memory (ROM)

• Types of ROM
  • Mask Programmable, aka, ROM
    • Key characteristics
      • Not practical for small quantities
      • Only used if a very large number of ROMs of a specific type is needed
        • Character Generators for CRTs
        • Mathematical tables
  • Disadvantages
    • If there is a design change the current stock cannot be reprogrammed
  • Advantages
    • For very large production runs the ROMs can be very inexpensive
    • In high security environments the programs on ROMs cannot be hacked and changed
Read Only Memory (ROM)

• Types of ROM
  • Programmable ROMs, aka, PROM
    • Key characteristics
      • User Programmable after manufacture
      • Uses fusible links
        • All links are in-place after manufacture
      • Cannot be reprogrammed
        • Fuses are selectively blown during the programming process
  • Programming Process
    • The desired binary address is placed on the address pins
    • The desired binary data is placed on the input pins
    • A high voltage (10 – 30 V) pulse is applied to a programming pin
      • A relatively high current flows through the memory cells that have 0V on their inputs
      • The fuse melts/blows. That memory cell is permanently at a LOW
Read Only Memory (ROM)

• **Types of ROM**
  • **Programmable ROMs, aka, PROM**
    • **Disadvantages**
      • Cannot be reprogrammed
    • **Advantages**
      • Reliability
      • Stores data permanently
      • Moderate price
      • Built using integrated circuits, rather than discrete components.
      • Fast: speed is between 35ns and 60ns.
  • **Erasable Programmable ROMs, aka, EPROM**
    • **Key characteristics**
      • User Programmable after manufacture
      • User erasable
        • 15 – 20 Minutes of intense UV Light
Read Only Memory (ROM)

Types of ROM

- Erasable Programmable ROMs, aka, EPROM
  
  Key characteristics
  
  - User erasable
    
    - UV light enters chip through the small quarts window
    
    - Photo electric process resets the memory cells to all Logic 1s
  
  - A programmed EPROM retains its data for about ten to twenty years and can be read an unlimited number of times.

  Sizes from
  
  - 256 – 1 million bytes

Disadvantages

- The erasing window must be kept covered with a foil label to prevent accidental erasure by sunlight.

- Reprogramming time slows developmental testing

- Leaving the erasing window of such a chip exposed to light can also change behavior
Read Only Memory (ROM)

• Types of ROM
  • Erasable Programmable ROMs, aka, EPROM
    • Advantages
      • User erasable
      • For security control:
        • Physical access and 15 – 20 minutes per EPROM is required to reprogram them
        • Also special equipment is required
  • Electrically Erasable Programmable ROMs, aka, EEPROM
    • Characteristics
      • Also called an E²PROM
      • User erasable electrically UV light sources aren’t required
      • Usually used in computers and other devices to store small amounts of volatile (configuration) data
Read Only Memory (ROM)

• **Types of ROM**
  
  • **Electrically Erasable Programmable ROMs, aka, EEPROM**
    
    • **Characteristics**
      
      • There are two major categories of the different types of electrical interfaces to EEPROM devices.
        
        • Serial bus
        • Parallel bus
      
      • **Serial bus**
        
        • Limited number of inputs the control, address, and data signals time share the inputs
      
      • **Parallel bus**
        
        • Has separate parallel control, address, and data inputs
        • Much faster than the serial bus versions
Read Only Memory (ROM)

• Types of ROM
  • Electrically Erasable Programmable ROMs, aka, EEPROM
    • Disadvantages
      • Can only hold small amounts of data
      • When larger amounts of static data are to be stored other memory types like flash memory (such as in USB flash drives) are more economical.
      • For security protection: can be electrically erased – without physical access
    • Advantages
      • Can be electrically erased – without physical access
      • Economical for storing small amounts of static data
Random Access Memory (RAM)

• Overview of RAM
  • Semiconductor memory in which specific contents can be accessed (read or written) directly by the CPU
    • Quick access regardless of the sequence (and hence location) in which they were recorded.
  • Two types of memory are possible with random-access circuits,
    • static RAM (SRAM)
      • Each memory cell stores a binary digit (1 or 0) for as long as power is supplied.
    • dynamic RAM (DRAM).
      • The charge on individual memory cells must be refreshed periodically in order to retain data.
      • Because it has fewer components, DRAM requires less chip area than SRAM;
      • Its access time is slower.
Random Access Memory (RAM)

• Overview of RAM
  • A single memory chip is made up of several million memory cells.

• Ram Architecture
  • Capacities
    • Sizes are stated in terms of bytes stored
    • Range from 1kB, 4kB, 8kB, 16kB, 64kB, 128kB, 256kB, 1MB, and much higher
      • Word sizes range from 1, 4, 8 bits
      • e.g., 2GB DDR SDRAM for PCs
        • Would require 8 256MB chips
  • Following figure shows a simplified RAM architecture
    • It holds 64 4-bit words (a 64X4 memory)
    • Address range from 0 – 63₁₀ 000000 – 11111₁₂
      • Requires 6-address lines – one for each bit of the address
      • Requires 4 data lines one for each bit of the data word
Radom Access Memory (RAM)

- Ram Architecture
Radom Access Memory (RAM)

- Ram Architecture
  - The figure shows a simplified RAM architecture
    - Each address code activates one particular decoder output
    - Each decoder output enables only the corresponding register
- Read Operation
  - The address code picks out one register in the memory chip for reading.
    - In order to read the contents of the selected register, the READ/WRITE (R/W) input must be a 1.
- Control Signals
  - CHIP SELECT (/CS) input must be active.
  - $R/W = 1$ and $/CS = 0$ enables the output buffers so that the contents of the selected register will appear at the four data outputs.
  - $R/W = 1$ also disables the input buffers so that the data inputs do not affect the memory during a read operation.
Radom Access Memory (RAM)

• Ram Architecture
  • Write Operation
    • The address code picks out one register in the memory chip for Writing.
      • In order to write the contents of the selected register, the READ/WRITE (R/W) input must be a 0.
  • Control Signals
    • CHIP SELECT (/CS) input must be active.
    • R/W = 0 and /CS = 0.
      • This combination enables the input buffers so that the four-bit word applied to the data inputs will be loaded into the selected register.
    • The R/W = 0 also disables the output buffers, which are tristate, so that the data outputs are in their Hi-Z state during a write operation.
    • The write operation destroys the word that was previously stored at that address.
Ram Architecture

• Chip Select
  • Most memory chips have one or more CS inputs which are used to enable the entire chip or disable it completely. In the disabled mode all data inputs and data puts are disabled.

• Common Input/Output Pins
  • In order to conserve pins on an IC package, manufacturers often combine the data input and data output functions using common input/output pins.
    • The R/W input controls the function of these I/O pins.
    • During a read operation, the I/O pins act as data outputs which reproduce the contents of the selected address location.
    • During a write operation, the I/O pins act as data inputs to which the data to be written are applied.

Random Access Memory (RAM)
Random Access Memory (RAM)

- **Ram Architecture**
  - Sample circuit to select and use RAM